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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,363	10/02/2000	Scott B. Swaney	POU920000162US1	6279

7590 09/11/2003

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EXAMINER	
GERSTL, SHANE F	
ART UNIT	PAPER NUMBER
2183	4

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,363	SWANEY ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/5/01, 12/22/00, and 10/02/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-22 have been examined.

Papers Received

2. Receipt is acknowledged of Information Disclosure Statement and Formal Drawing papers where the papers have been placed of record in the file.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claim 1 is objected to because of the following informalities: the phrase "said determining a valid match" of line 9 is unclear. The examiner is taking this phrase to mean: "said determining produces a valid match."

5. Claim 6 is objected to because of the following informalities: the singular indefinite article, "a", is used in conjunction with a plural noun, "addresses". The examiner is interpreting the claim to have the mentioned "a" removed from the claim language since it is required that multiple addresses exist if one is to compare them.

6. Claims 8 and 9 objected to because of the following informalities: the word "interlocks" is plural, however there is possibility of there being only one interlock as stated in claim 1.

7. Claims 8 and 19 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s)

in proper dependent form, or rewrite the claim(s) in independent form. Claim 8 simply restates line 9 of parent claim 1 and claim 19 restates lines 7 and 8 of claim 12.

8. Claims 4 and 15 are objected to because of the following informalities: the singular indefinite article, "an", is used in conjunction with a plural noun, "addresses". The examiner is interpreting the word "addresses" to mean "address" in the singular based on the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-11, 21, and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. In claim 1 it is unclear whether the addresses of mention in line 2 are the same as the R-unit register addresses in line 3 or not even though it is implied. The examiner is taking these two different address types to in fact be the same based on the specification. It is also unclear based on the claim language whether the R-unit operands of mention in line one are the same as the R-unit addresses in line 3. The examiner is taking the R-unit operands to be the actual contents of the register rather than the register addresses.

12. Claims 2-11 are rejected on the same basis as claim 1 because they are each dependent claims of parent claim 1 and thus inherit all the properties and faults of it.

13. Claim 10 recites the limitation "said write queue" in line 1. There is insufficient antecedent basis for this limitation in the claim. Parent claim 1 makes no mention of a write queue. The examiner will interpret the statement as meaning, "a write queue."

14. Claim 11 recites the limitation "said write queue" in line 2. There is insufficient antecedent basis for this limitation in the claim. Parent claim 1 makes no mention of a write queue. The examiner will interpret the statement as meaning, "a write queue."

15. Claim 21 recites the limitation "said updating" in line 1. There is insufficient antecedent basis for this limitation in the claim. Parent claims 12 and 14 make no claim of a method for updating. The examiner is taking the claim to mean, "The system in claim 14 wherein it is allowed for R-unit register addresses to accumulate in said write queue."

16. Claim 22 recites the limitation "said R-unit" in line 1. There is insufficient antecedent basis for this limitation in the claim. Parent claims 12 and 14 are not claiming an R-unit, but only operands and addresses that can be used in conjunction with one. Therefore, the claim also does not further limit the parent claim.

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-3, 5-6, 7-10, 12-14, 16, and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Edmondson et al. (5,471,591).

19. In regard to claim 1, Edmondson discloses a method for holding up R-unit operands for a minimum number of cycles until all prior updates have completed by comparing R-unit register addresses in at least one queue and interlocking valid R-unit register address matches, the method comprising:

a. receiving a plurality of R-unit register addresses; Note column 4, line 29, where Edmondson mentions register specifiers. One of ordinary skill in the art would recognize these specifiers to be an address of sorts because it points to a specific register.

b. storing said R-unit register addresses in a plurality of queues; Note that in column 4, lines 24-25, Edmondson stores his register (source and destination) specifiers (addresses) in queues.

c. accessing said queues; Note in column 4, lines 40-41, that Edmondson inspects said queues. It is well known in the art that in order to inspect a queue it must be accessed.

d. comparing said R-unit register addresses; Note in column 5, lines 9-12, that Edmondson compares a register destination specifier to a register source specifier. It has already been shown that specifier means an address.

e. determining matches between R-unit register addresses; In column 5, lines 40-41, Edmonson discloses that the comparators indicate a match. It has already been shown above that the comparators compare register addresses.

f. implementing one or more interlocks after said determining a valid match. In column 5, lines 40-41 Edmondson shows that if there is a match, the current

instruction is stalled. It is well known to one of ordinary skill in the art that this stall is in fact an interlock.

20. In regard to claim 2, Edmondson discloses the method of claim 1 wherein said interlock causes a read instruction not to execute in column 28, lines 43-47, where as shown previously, the stall is the interlock.

21. In regard to claim 3, Edmondson discloses the method of claim 1 wherein said plurality of queues includes a write queue (column 27, line 61, destination queue), pre-write queue (prefetch queue) and a read queue (column 27, line 60, source queue). The pre-write queue is disclosed as a prefetch queue (column 26, line 64). This queue holds register addresses (identifiers) that are later sent to the write queue (Figure 7, elements 38 and 69; column 27, lines 42-49), hence it acts as a pre-write queue.

22. In regard to claims 5, Edmondson discloses the method of claim 3 wherein said comparing includes comparing said R-unit register addresses sent to said read queue against said R-unit register addresses sent to said write queue (column 5, line 9-12, destination and source specifiers).

23. In regard to claim 6, Edmondson discloses the method in claim 3 wherein said determining includes matching valid R-unit register addresses of said write queue and read queue (column 5, line 9-12, destination and source specifiers). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

24. In regard to claim 7, Edmondson discloses the method in claim 3 wherein said determining includes matching valid R-unit register addresses of said pre-write queue and read queue (column 5, line 9-12, destination and source specifiers). The pre-write

queue information acts as the destination specifier in this case as it will be written and is an input to the read queue (Figure 7, operand bus). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

25. In regard to claim 8, Edmondson discloses the method in claim 1 wherein said interlocks are implemented after said R-unit register address match is determined. (column 5, lines 40-41, the stall is an interlock).

26. In regard to claim 9, Edmondson discloses the method of claim 1 wherein said interlocks prevent read instructions from being processed (column 28, lines 43-47, stalls).

27. In regard to claim 10, Edmondson discloses the method in claim 1 wherein said write queue accumulates R-unit register addresses (column 4, lines 51-52, register destination specifiers).

28. In regard to claim 12, Edmondson discloses a system for holding up R-unit operands for a minimum number of cycles until all prior updates have completed by comparing R-unit register addresses in at least one queue and interlocking valid R-unit register address matches, the system comprising:

a. a plurality of queues for storing R-unit register addresses (Figure 7, elements 37 and 38);

b. a comparator for comparing said R-unit register addresses in said plurality of queues and determining matches between R-unit register addresses (Figure 18, element 641); and

c. a plurality of interlocks that are implemented after determining valid matches of said R-unit register addresses (column 5, lines 40-41, the stalling is an interlock).

29. In regard to claim 13, Edmondson discloses the system of claim 12 wherein one of said interlocks causes a read instruction not to execute (column 28, lines 43-47, stalls).

30. In regard to claim 14, Edmondson discloses the system of claim 12 wherein said plurality of queues includes a write queue (Figure 7, element 38), pre-write queue (Figure 7, element 69) and a read queue (Figure 7, element 37). The pre-write queue is disclosed as a prefetch queue (column 26, line 64). This queue holds register addresses (identifiers) that are later sent to the write queue (column 27, lines 42-49); hence it acts as a pre-write queue.

31. In regard to claims 16, Edmondson discloses the system of claim 14 wherein said comparator compares said R-unit register addresses sent to said read queue against said R-unit register addresses sent to said write queue (Figure 18, element 641).

32. In regard to claim 19, Edmondson discloses the system in claim 13 wherein said interlocks are implemented after said valid R-unit register address match is determined (column 5, lines 40-41, the stalling is an interlock).

33. In regard to claim 20, Edmondson discloses the system of claim 13 wherein said interlocks prevent read instructions from being processed (column 28, lines 43-47, stalls).

34. In regard to claim 21, Edmondson discloses the method in claim 14 wherein said updating allows R-unit register addresses to accumulate in said write queue (column 4, lines 51-52, register destination specifiers).

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 4, 11, 15, 17, and 18, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edmondson in view of Hennessy.

37. In regard to claim 4:

a. Edmondson discloses the method of claim 3 as described above in paragraph 21.

b. Edmondson's disclosure lacks the addition of a method where a bypass sends an R-unit register address when said read queue is empty.

c. Hennessy teaches that bypassing or forwarding is used to get an item early in order to avoid waiting for the item and speed up the system process (page 445, bottom paragraph). When Edmonson's read queue is empty, the incoming address is stored and then sent out right away. Placing register addresses into the read queue and removing them cost valuable cycle time. It would have been desirable to be able to avoid this added delay of the queue when it is not necessary.

d. The ability to be able to avoid any delay associated with the read queue when possible would have motivated one of ordinary skill in the art to bypass the read queue when it is empty.

It would have been obvious to one of ordinary skill in the art at the time of invention to use a method wherein a bypass sends an R-unit register address when said read queue is empty in order to avoid the delays of the read queue.

38. In regard to claim 11:

a. Edmondson discloses all the features of claim 1 as described in paragraph 19 above. Edmondson also teaches that the write queue accumulates results as shown in paragraph 27 above.

b. Edmondson does not disclose that an SRAM is used to receive the accumulated results from said write queue.

c. Hennessy teaches that SRAM is the technology of choice for registers. Edmondson's disclosed invention writes the results in the write queue to registers. Hennessy teaches that it is desirable to use faster memory closer to the processor (page 541, bottom paragraph). Registers are memory close to the processor. SRAM is the fastest standard type of memory in terms of access time as shown by Hennessy in the table on page 541.

d. The quick access time achieved by the use of SRAM technology for the registers that the write queue sends data to would have motivated one of ordinary skill in the art to use SRAM as the memory system of choice for the registers disclosed in Edmondson.

It would have been obvious to one of ordinary skill in the art at the time of invention to use SRAM technology to implement the registers disclosed by Edmondson in order to improve the access time of the registers.

39. In regard to claim 15:

a. Edmondson discloses the system of claim 14 as described above in paragraph 30.

b. Edmondson's disclosure lacks the addition of a bypass that sends an R-unit register address when said read queue is empty.

c. Hennessy teaches that bypassing or forwarding is used to get an item early in order to avoid waiting for the item and speed up the system process (page 445, bottom paragraph). When Edmonson's read queue is empty, the incoming address is stored and then sent out right away. Placing register addresses into the read queue and removing them cost valuable cycle time. It would have been desirable to be able to avoid this added delay of the queue when it is not necessary.

d. The ability to be able to avoid any delay associated with the read queue when possible would have motivated one of ordinary skill in the art to bypass the read queue when it is empty in order to avoid the delays of the read queue.

It would have been obvious to one of ordinary skill in the art at the time of invention to use a bypass that sends an R-unit register address when said read queue is empty in order to avoid the delays of the read queue.

40. In regard to claim 17, Edmondson discloses the system in claim 15 as described above in paragraph 39 wherein said determining includes matching valid R-unit register addresses of said write queue and read queue (column 5, line 9-12, destination and source specifiers). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

41. In regard to claim 18, Edmondson discloses the system in claim 15 wherein said comparator determines said valid R-unit register address matches between said pre-write queue and said read queue (column 5, line 9-12, destination and source specifiers). The pre-write queue information acts as the destination specifier in this case and is an input to the read queue (Figure 7, operand bus). Edmondson also teaches that the addresses (specifiers) must be valid (column 20, lines 33-35).

42. In regard to claim 22:

a. Edmondson discloses all the features of claim 14 as described in paragraph 30 above. Edmondson also teaches that the write queue accumulates results as shown in paragraph 27 above.

b. Edmondson does not disclose that an SRAM is used to receive the accumulated results from said write queue.

c. Hennessy teaches that SRAM is the technology of choice for registers. Edmondson's disclosed invention writes the results in the write queue to registers. Hennessy teaches that it is desirable to use faster memory closer to the processor (page 541, bottom paragraph). Registers are a memory

close to the processor. SRAM is the fastest standard type of memory in terms of access time as shown by Hennessy in the table on page 541.

d. The quick access time achieved by the use of SRAM technology for the registers that the write queue sends data to would have motivated one of ordinary skill in the art to use SRAM as the memory system of choice for the registers disclosed in Edmondson.

It would have been obvious to one of ordinary skill in the art at the time of invention to use SRAM technology to implement the registers disclosed by Edmondson in order to improve the access time of the registers.

Conclusion

43. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the art with respect to interlocks and keeping track of register identifiers:

US Pat No 4,903,196 to Pomerene shows the use of destination and source queues to maintain data integrity.

US Pat No 5,251,306 to Tran shows the use of scoreboarding in order to indicate how each register is being used by a plurality of instructions.

US Pat No 6,438,681 B1 to Arnold shows the use of comparison logic with decoded register identifiers to detect data hazards.

US Pat No 5,790,827 to Leung shows a dependency checking method using a scoreboard.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
September 4, 2003

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